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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/080,578	02/25/2002	Hiroshi Hatae	ASAM.0045	8728

7590 09/09/2005

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EXAMINER	
LI, AIMEE J	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 09/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/080,578	HATAE ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 18-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 18-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-5 and new claims 18-24 have been considered. Claims 1-4 have been amended as per Applicant's request. Claims 6-17 have been withdrawn as per Applicant's request. New claims 18-24 have been added as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received on 22 June 2005 and Extension of Time for 3 Months as received on 22 June 2005.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-5 and 18-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gove et al., U.S. Patent Number 5,212,777 (herein referred to as Gove) in view of Wise, U.S. Patent Number 5,978,592 (herein referred to as Wise).

5. Referring to claim 1, Gove has taught a semiconductor integrated circuit, comprising:

a. A single instruction multiple data (SIMD) unit conducting a concurrent operation of data items for a plurality (Gove column 1, line 50 to column 2, line 5; column 3, lines 5-13; column 5, lines 20-47; column 6, lines 6-12; Figure 1; and Figure 2);

b. A data buffer connectible to said SIMD unit (Gove column 5, lines 20-47; column 6, lines 23-36; column 16, lines 6-17; Figure 1; Figure 2; and Figure 16); and

c. A data transfer control unit for controlling transfer of data for said data buffer (Gove column 2, lines 47-53; column 2, line 62 to column 3, line 13; column 5, lines 35-48; column 12, lines 32-56; column 16, lines 6-17; Figure 1; Figure 2; Figure 17; and Figure 57),

6. Wherein said data transfer control unit controls the transfer of data for a subsequent operation to said data buffer in concurrence with the operation of said SIMD unit for the plural data items read from said data buffer (Gove column 2, lines 47-53; column 2, line 62 to column 3, line 13; column 5, lines 35-48; column 12, lines 32-56; column 16, lines 6-17; Figure 1; Figure 2; Figure 17; and Figure 57). In regards to Gove, Gove has taught that the transfer processor is autonomous from the SIMD processing area and feeds data into data buffer locations that are not in use by the SIMD.

7. Gove has not taught wherein said data transfer control unit controls transfer of data for a subsequent operation to said data buffer from outside of said semiconductor integrated circuit in concurrence with the current operation for a plurality of data items read from said data buffer. Wise has taught wherein said data transfer control unit controls transfer of data for a subsequent operation to said data buffer from outside of said semiconductor integrated circuit in concurrence with the current operation for a plurality of data items read from said data buffer (Wise column 248, lines 44-53; column 249, lines 1-6; Figure 24; and Figure 131). A person of ordinary skill in the art at the time the invention was made would have recognized that having a double buffer allows data to be read and written at the same time from the buffering area, thereby increasing

processor speed, since read and write operations are done concurrently. Therefore, it would have been obvious to a person of ordinary skill in the art the time the invention was made to incorporate the double buffer of Wise in the device of Gove to increase processor speed.

8. Referring to claim 2, Gove has taught wherein said data buffer includes a dual-port unit including a first port and a second port (Gove column 6, lines 47-58; column 7, lines 5-13; column 12, lines 32-56; column 16, lines 6-17; Figure 1; Figure 2; Figure 4; Figure 17; and Figure 57),

a. Said first port being connected via a first bus to said SIMD unit (Gove column 6, lines 47-58; column 7, lines 5-13; column 12, lines 32-56; column 16, lines 6-17; column 37, lines 5-20; Figure 1; Figure 2; Figure 4; Figure 17; Figure 30; and Figure 57),

b. Said second port being connected via a second bus to said data transfer control unit (Gove column 6, lines 47-58; column 7, lines 5-13; column 12, lines 32-56; column 16, lines 6-17; column 59, line 45 to column 60, line 3; Figure 1; Figure 2; Figure 4; Figure 17; and Figure 57). In regards to Gove, the port is inherent to the Transfer Processor in order for it to receive and transmit data.

9. Referring to claim 3, Gove has taught

a. Said first port concurrently input and output the plurality of data items for said first bus (Gove column 6, lines 47-58; column 7, lines 5-13; column 12, lines 32-56; column 16, lines 6-17; column 37, lines 5-20; Figure 1; Figure 2; Figure 4; Figure 17; Figure 30; and Figure 57); and

b. Said second port concurrently input and output the plurality of data items for said second bus (Gove column 6, lines 47-58; column 7, lines 5-13; column 12, lines 32-56; column 16, lines 6-17; column 59, line 45 to column 60, line 3; Figure 1; Figure 2; Figure 4; Figure 17; and Figure 57).

10. Referring to claim 4, Gove has taught

a. A first data register connected to said first bus, said first data register being concurrently latched the plurality of data items (Gove column 38, lines 9-12; column 39, lines 11-35; Figure 30; and Figure 32);

b. A second data register connected to said first bus, said second data register being concurrently latched the plurality of data items (Gove column 38, lines 9-12; column 39, lines 11-35; Figure 30; and Figure 32);

c. An operator for receiving the plurality of data items respectively latched by said first and second data registers and for conducting a concurrent operation for the data items (Gove column 38, lines 9-12; column 39, lines 11-35; Figure 30; and Figure 32).

11. Referring to claim 5, Gove has taught a central processing unit conducting operation control for said SIMD unit and access control via said first bus to said data buffer (Gove column 5, lines 35-47; column 6, lines 23-25; column 12, line 59 to column 13, line 9; column 35, lines 36-49; Figure 1; Figure 2; Figure 4; Figure 17; Figure 29; and Figure 67).

12. Referring to claims 18-24, Gove has taught doing operations in a concurrent manner (Applicant's claim 20) (Gove column 1, line 50 to column 2, line 5; column 4, lines 5-13; column 5, lines 20-47; column 6, lines 6-12; Figure 1; and Figure 2). Gove has not taught

a. Wherein said data transfer control unit includes a bit extension unit for conducting bit extension for each of said plurality of data items transferred via said second bus to said data buffer (Applicant's claim 18).

b. Wherein said bit extension unit conducts 1-bit code extension according to a lower-mist bit of said plurality of data items (Applicant's claim 19).

c. Wherein said bit extension unit conducts bit extension for said plurality of data items in a concurrent fashion (Applicant's claim 20).

d. A data aligner in a stage before said bit extension unit for said plurality of data items (Applicant's claim 21).

e. Wherein said data transfer control unit includes a bit removal unit for removing bits from each of said plurality of data items which are used from said data buffer and which are transferred via said second bus (Applicant's claim 22).

f. Wherein said bit removal unit removes a higher-most bit from said plurality of data items (Applicant's claim 23).

g. Wherein said first and second data registers latch image data when being in compression processing of image data (Applicant's claim 24), and

h. Wherein said first data register latches image data and said second data register latches data of inverse discrete cosine transform (IDCT) when being in expansion of image data (Applicant's claim 24).

13. Wise has taught

a. Wherein said data transfer control unit includes a bit extension unit for conducting bit extension for each of said plurality of data items transferred via said second

bus to said data buffer (Applicant's claim 18) (Wise column 27, lines 42-53 and column 54, line 66 to column 55, line 5).

b. Wherein said bit extension unit conducts 1-bit code extension according to a lower-most bit of said plurality of data items (Applicant's claim 19) (Wise column 27, lines 42-53 and column 54, line 66 to column 55, line 5).

c. Wherein said bit extension unit conducts bit extension for said plurality of data items (Applicant's claim 20) (Wise column 27, lines 42-53 and column 54, line 66 to column 55, line 5).

d. A data aligner in a stage before said bit extension unit for said plurality of data items (Applicant's claim 21) (Wise column 75, lines 11-15 and column 132, lines 36-43).

e. Wherein said data transfer control unit includes a bit removal unit for removing bits from each of said plurality of data items which are used from said data buffer and which are transferred via said second bus (Applicant's claim 22) (Wise column 248, lines 44-53; column 249, lines 1-6; and Figure 131). In regards to Wise, reading data from the double buffer removes bits from the buffer.

f. Wherein said bit removal unit removes a higher-most bit from said plurality of data items (Applicant's claim 23) (Wise column 248, lines 44-53; column 249, lines 1-6; and Figure 131). In regards to Wise, reading data from the double buffer removes bits from the buffer, including the higher-most bit.

g. Wherein said first and second data registers latch image data when being in compression processing of image data (Applicant's claim 24) (Wise column 36, line 57 to column 37, line 5 and Figure 19), and

h. Wherein said first data register latches image data and said second data register latches data of inverse discrete cosine transform (IDCT) when being in expansion of image data (Applicant's claim 24) (Wise column 36, line 57 to column 37, line 5; column 74, lines 60-67; and Figure 19).

14. A person of ordinary skill in the art, and as taught by Wise, would have recognized that all these traits improve the flexibility, efficiency and performance of a graphics processing system using video compression/decompression (Wise column 6, lines 8-13). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the bit extension and double buffering of Wise in the device of Gove to improve the flexibility, efficiency and performance.

Response to Arguments

15. Examiner withdraws the 35 U.S.C. 112, first paragraph rejection of claim 3 in favor of the amended claims.

16. Applicant's arguments with respect to claims 1-5 and 18-24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

17. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

18. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

20. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

21. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL

Aimee J. Li
5 September 2005

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